

IN THE CLAIMS:

Following are claims in the elected Group I responsive to the Examiner's restriction requirement:

1. (Original) A method, comprising:
executing an instruction that updates data in a register at a first time;
marking the instruction as a slowable instruction when the data is not
read from the register at a next clock cycle from completion of
execution of the instruction.
2. (Original) The method of claim 1, further comprising:
storing an instruction address of the instruction.
3. (Original) The method of claim 2, further comprising:
when the instruction is marked as a slowable instruction, using the stored
instruction address to store an entry indicating that the instruction is slowable.
4. (Original) The method of claim 3, further comprising:
when the instruction address of the instruction is encountered a
second time and the instruction is marked as a slowable instruction, delaying
processing of the instruction.
5. (Original) The method of claim 4, wherein when the instruction address of the
instruction is encountered the second time, the stored entry is used to
determine if the instruction is slowable.
6. (Original) The method of claim 4, wherein delaying the processing of the
instruction comprises delaying decoding the instruction.

7. (Original) The method of claim 4, wherein delaying the processing of the instruction comprises using lower priority resources to execute the instruction.

8. (Original) The method of claim 4, wherein delaying the processing of the instruction comprises delaying loading the data into the register until prior to the data is read from the register.

9. (Original) A method, comprising:

recording a first clock cycle when an instruction that loads data into a register is to complete;

recording a second clock cycle when the data is read from the register; and

making the instruction as a slowable instruction when the second clock cycle is more than a predetermined time threshold from the first clock cycle.

10. (Original) The method of claim 9, wherein the predetermined time threshold is at least one clock cycle.

11. (Original) The method of claim 9, further comprising:

storing an instruction address of the instruction at a first time.

12. (Original) The method of claim 11, further comprising:

when the instruction is marked as a slowable instruction, using the stored instruction address to store an entry indicating that the instruction is slowable.

13. (Original) The method of claim 12, wherein when the instruction address of the instruction is loaded into an instruction pointer at a second time, the stored entry is used to determine if the instruction is slowable.

14. (Original) The method of claim 13, wherein when the instruction is determined to be slowable, processing of the instruction is delayed.
15. (Original) The method of claim 14, wherein the processing of the instruction is delayed by delaying decoding the instruction.
16. (Original) The method of claim 14, wherein the processing of the instruction is delayed by using lower priority resources to execute the instruction.
17. (Original) The method of claim 9, wherein information about the first clock cycle and the second clock cycle is provided by a scheduler.
18. (Original) The method of claim 17, wherein the scheduler provides the information about the first clock cycle and the second clock cycle prior to execution of the instruction.
19. (Original) A computer readable medium having stored thereon sequences of instructions which are executable by a system, and which, when executed by the system, cause the system to perform a method, comprising:
executing an instruction that loads data into a register at a first time; and
marking the instruction as a slowable instruction when the data is not read from
the register at a next clock cycle from completion of execution of
the instruction.
20. (Original) The computer readable medium of claim 19, further comprising:
storing an instruction address of the instruction.

21. (Original) The computer readable medium of claim 20, further comprising:
when the instruction is marked as a slowable instruction, using the
stored instruction address to store an entry indicating the instruction is slowable.

22. (Original) The computer readable medium of claim 21, further comprising;
when the instruction address of the instruction is encountered a second time and
the instruction is marked as a slowable instruction, delaying processing of the
instruction.

23. (Original) The computer readable medium of claim 22, wherein when the
instruction address of the instruction is encountered the second time, the stored
entry is used to determine if the instruction is marked as a slowable instruction.

24. (Original) The computer readable medium of claim 22, wherein delaying the
processing of the instruction comprises delaying decoding the instruction.

25. (Original) The computer readable medium of claim 22, wherein delaying the
processing of the instruction comprises using lower priority resources to execute
the instruction.

26. (Original) The computer readable medium of claim 22, wherein delaying the
processing of the instruction comprises delaying loading the data into the register
until prior to the data is read from the register.

27. (Original) A computer readable medium having stored thereon sequences of instructions which are executable by a system, and which, when executed by the system, cause the system to perform a method, comprising:

recording a first clock cycle when an instruction is to complete loading data in a register;

recording a second clock cycle when the data is read from the register; and

making the instruction as a slowable instruction when the second clock cycle is more than a predetermined time threshold from the first clock cycle.

28. (Original) The computer readable medium of claim 27, wherein the predetermined time threshold is at least one clock cycle.

29. (Original) The computer readable medium of claim 27, further comprising: storing an instruction address of the instruction at a first time.

30. (Original) The computer readable medium of claim 29, further comprising: when the instruction is marked as a slowable instruction, using the stored instruction address to store an entry indicating that the instruction is a slowable instruction.

31. (Original) The computer readable medium of claim 30, wherein when the instruction address of the instruction is loaded into an instruction pointer at a second time, the stored entry is used to determine if the instruction is a slowable instruction.

32. (Original) The computer readable medium of claim 31, wherein when the instruction is determined to be slowable, processing of the instruction is delayed.

33. (Original) The computer readable medium of claim 32, wherein the processing of the instruction is delayed by delaying decoding the instruction.

34. (Original) The computer readable medium of claim 32, wherein the processing of the instruction is delayed by using lower priority resources to execute the instruction.

35. (Original) The computer readable medium of claim 27, wherein information about the first clock cycle and the second clock cycle are provided by a scheduler.

36. (Original) The computer readable medium of claim 35, wherein the scheduler provides the information about the first clock cycle and the second clock cycle prior to execution of the instruction.